IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	:	10/785,648	Confirmation No. 3709
Applicant:	:	Timothy A. Rost	
Filed:	:	February 24, 2004	
Art Unit:	:	2814	
Examiner:	:	Long Pham	
Docket No.	:	TI-36595	
Customer No.	:	23494	

APPEAL BRIEF UNDER 37 C.F.R. 1.192

Mail Stop Appeal Brief - Patents
Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The following Appeal Brief is respectfully submitted in connection with the above identified application in response to the final rejection mailed January 23, 2006, and the Advisory Action mailed April 12, 2006.

Real Party in Interest under 37 C.F.R. 41.37(c)(1)(i)

Texas Instruments Incorporated is the real party in interest.

Related Appeals and Interferences under 37 C.F.R. 41.37 (c)(1)(ii)

There are no related appeals or interferences known to appellant, the appellant's legal representative, or assignee which will directly affect or be directly affected by or have a bearing on the board's decision in the pending appeal.

Status of Claims on Appeal under 37 C.F.R. 41.37 (c)(1)(iii)

Claims 1-8 and 19-23 were withdrawn and canceled. Claims 9 – 18 which are appealed are rejected.

Status of Amendments Filed After Final rejection under 37 C.F.R. 41.37 (c)(1)(iv)

An office action for reconsider was filed under 37 C.F.R. 1.116. The office action contained responses to an object of claim 9 under 35 U.S.C. 112 and a rejection to claims 9-18 under 35 U.S.C. 103(a). In response to the filed office action the rejection of claim 9 under 35 U.S.C. 112 was withdrawn. Regarding the rejection of claim 9-18 the office action was deemed NOT to place the application in condition for allowance.

Summary of the Invention under 37 C.F.R. 41.37(c)(1)(v)

Shown in Figure 8 is a top view of a semiconductor wafer with NMOS and PMOS transistors. As described on page 9, line 13 the NMOS devices are formed oriented along a <100> crystallographic orientation axis such that the electron mobility is improved by applying a longitudinal tensile strain along the axis during fabrication (page 9, lines 10-19). The PMOS transistors are formed along a <110> crystallographic orientation axis such that the hole mobility is improved by applying a longitudinal compressive strain along this axis during fabrication (page 9, lines 20-26). One way to achieve this is by laying out the NMOS devices at a non-parallel offset angle from the axis employed by the PMOS devices (45 degrees). This permits the NMOS and PMOS devices to be fabricated within the same semiconductor substrate unlike other mechanisms or solutions that require etching away some of the substrate and depositing other substrate material to fabricate devices within (page 10, lines 1-9). Shown in Figure 9 and described starting on page 10, line 27 is a method for forming the NMOS and PMOS transistors of the instant invention.

Statement of Issues Presented for Review under 37 C.F.R. 41.37 (c)(1)(vi)

Are claims 9-19 properly rejected under 35 U.S.C. 103(a) as being unpatentable over Ouyang et al. (US Publication 2004/0256639) in combination with Lin et al. (US Publication 2005/0035369), Yeo et al. (US Publication 2005/009263), Chidambarrao et al. (US publication 2005/0164477), and Curie et al. (US Publication 2004/0173812)?

Argument under 37 C.F.R. 41.37(c)(1)(vii)

(1) Claims 9-18 not properly rejected under 35 U.S.C. 103(a) as being unpatentable over Ouyang et al. (US Publication 2004/0256639) (Ouyang) in combination with Lin et al. (US Publication 2005/0035369) (Lin), Yeo et al. (US Publication 2005/009263) (Yeo), Chidambarrao et al. (US publication 2005/0164477) (Chidambarrao), and Curie et al. (US Publication 2004/0173812) (Curie) ?

In forming the rejection the Examiner argues that Ouyang in combination with Lin, Yeo, Chidambarrao, and Curie teach forming the vertical MOS having the source, drain channel formed above the substrate but fails to teach that the MOS is a lateral MOS or MOS having source, drain and channel formed in the substrate. The Examiner than concludes that it would have been obvious to one of ordinary skill in the art of making semiconductor devices to form the source, drain and channel in the substrate to form a lateral MOS transistor having high channel mobility.

As stated in specification of the instant invention the method of the instant invention permits the NMOS and PMOS devices to be fabricated within the same semiconductor substrate unlike other mechanisms or solutions that require etching away some of the substrate and depositing other substrate material to fabricate devices within (page 10, lines 1-9). As stated by the Examiner the cited references teach forming the vertical MOS having the source, drain channel formed above the substrate but fails to teach that the MOS is a lateral MOS or MOS having source, drain and channel formed in the substrate. The vertical MOS described by the Examiner is the very structure that the instant specification described as other mechanisms or solutions that require etching away some of the substrate and depositing other substrate material to fabricate devices within (page 10, lines 1-9). The methods described in the combined references cannot produce the claimed invention if applied to forming lateral MOS devices. The combined references provide no mechanism to obtain the required conditions for improved mobility in both the NMOS and PMOS devices. In fact the methods described in the combined references cannot form lateral MOS transistors.

A prima facie case of obviousness requires that the cited references teach or suggest all of the claim limitations and also that some suggestion or motivation to combine the references be available. As described above, the combined references do not teach or suggest all of the claim limitations. In addition, not only is there no motivation to combine the references but the Ouyang reference teaches away from the limitations of the claimed invention. The Summary of the Ouyang reference teaches away from forming lateral MOS transistors by stating that it is not practical to integrate a nMOSFET on a (100) plane and a pMOSFET on a (110) plane using conventional silicon technology, but it is easy to do so with vertical devices [0015]. Without a proper motivation to combine the references the rejection is improper.

Conclusion

For the foregoing reasons, Appellant respectfully submits that the Examiner's final rejection of Claims 9-18 under 35 U.S.C. § 103 is not properly founded in law, and it is respectfully requested that the Board of Patent Appeals and Interferences so find and reverse the Examiner's rejections.

To the extent necessary, the Appellant petitions for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,

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APPENDIX

Claims on Appeal under 37 C.F.R. 41.37(c)(1)(viii)

Claim 9: A method of fabricating a semiconductor device comprising:

forming PMOS devices on a semiconductor substrate with source regions, drain regions, and entire source to drain channel regions formed within the substrate along a first crystallographic orientation axis of the semiconductor substrate;

forming NMOS devices on the semiconductor substrate with source regions, drain regions, and entire source to drain channel regions formed within the substrate rotated by an offset angle from the source to drain channel regions of the PMOS devices to lie along a second crystallographic orientation axis of the semiconductor substrate;

applying a compressive strain longitudinally across the source to drain channel regions of the PMOS devices to improve hole mobility; and

applying a tensile strain longitudinally across the source to drain channel regions of the NMOS devices to improve electron mobility.

Claim 10: The method of claim 9, wherein the crystallographic orientation axis on which the PMOS devices are formed is <110> and wherein the semiconductor substrate is silicon.

Claim 11: The method of claim 9, wherein the crystallographic orientation axis on which the NMOS devices are formed is <100>.

Claim 12: The method of claim 9, wherein the offset angle with which the source to drain channel region of the NMOS devices are formed is 45 degrees.

Claim 13: The method of claim 9, wherein applying the compressive strain longitudinally across the source to drain channel regions of the PMOS devices to improve hole mobility comprises applying uniaxial compressive strain.

Claim 14: The method of claim 9, wherein applying the compressive strain longitudinally across the source to drain channel regions of the PMOS devices to improve hole mobility comprises applying biaxial compressive strain.

Claim 15: The method of claim 9, wherein applying the compressive strain longitudinally across the source to drain channel regions of the PMOS devices to improve hole mobility comprises:

performing a recess etch of the source to drain channel regions; and

depositing a silicon-germanium epitaxial layer on the source to drain channel regions to introduce the compressive stress to the source to drain channel regions.

Claim 16: The method of claim 9, wherein applying the tensile strain longitudinally across the source to drain channel regions of the NMOS devices to improve electron mobility comprises applying biaxial tensile stress.

Claim 17: The method of claim 9, wherein applying the tensile strain longitudinally across the source to drain channel regions of the NMOS devices to improve electron mobility comprises:

performing a recess etch of the source to drain channel regions; and

depositing a carbon doped silicon layer on the source to drain channel regions to introduce the tensile stress to the source to drain channel regions.

Claim 18: The method of claim 9, wherein applying the tensile strain longitudinally across the source to drain channel regions of the NMOS devices to improve electron mobility comprises forming an interlayer dielectric layer over the NMOS devices to introduce the compressive stress to the source to drain channel regions.